IN THE CLAIMS

Replace the indicated claims with:

Sub C3

1. (Amended) A high-frequency semiconductor device comprising:

a substrate; and

an Si MOS transistor and a first lateral polysilicon diode on the substrate, the first lateral polysilicon diode having a forward direction and a reverse direction, wherein the first lateral polysilicon diode connects, in the forward direction, a high-frequency I/O signal line to an externally supplied voltage VDD.

A39

2. (Amended) The high-frequency semiconductor device of Claim 1, further comprising a second lateral polysilicon diode on the substrate and having a forward direction and a reverse direction, wherein the second lateral polysilicon diode connects, in the forward direction, ground, GND, to the high-frequency I/O signal line.

3. (Amended) The high-frequency semiconductor device of Claim 2, including m lateral polysilicon diodes connected in series between the high-frequency I/O signal line and the externally supplied voltage, VDD, and n lateral polysilicon diodes connected in series between the ground, GND, and the high-frequency I/O signal line wherein VDD/(n+m) is smaller than 1.1 volts.

4. (Amended) The high-frequency semiconductor device of Claim 1, wherein no lateral polysilicon diode is connected to any signal line other than the high frequency I/O signal line.

5. (Amended) The high-frequency semiconductor device of Claim 1 further comprising a capacitor having lower and upper polysilicon electrodes, wherein the first lateral polysilicon diode and the lower electrode of the capacitor are from a first polysilicon layer, and the MOS transistor has a polysilicon gate electrode from a second polysilicon layer.

Sub C3

6. (Amended) The high-frequency semiconductor device of Claim 1 further comprising a capacitor having lower and upper polysilicon electrodes, wherein the first lateral polysilicon diode and the lower electrode of the capacitor are from a first polysilicon layer, the MOS transistor has a polysilicon gate, and the upper electrode of the capacitor and the gate are from a second polysilicon layer.

A39

7. (Amended) The high-frequency semiconductor device of claim 5, wherein the polysilicon layer of the upper electrode of the capacitor covers a PN junction of the first lateral polysilicon diode.

8. (Amended) The high-frequency semiconductor device of claim 5, wherein the capacitor includes a dielectric layer and the dielectric layer covers a PN junction of the first lateral polysilicon diode.

9. (Amended) A method of manufacturing a high-frequency semiconductor device having a MOS transistor, lateral polysilicon diodes, and a capacitor on a substrate, and a first of the lateral polysilicon diodes connects a high-frequency I/O signal line to an externally supplied voltage, VDD, and a second of lateral polysilicon diodes connects ground, GND, to the high-frequency I/O signal line, the method comprising:

forming a first polysilicon layer and a lower electrode of the capacitor and the lateral polysilicon diodes from the first polysilicon layer:

forming a first dielectric layer as an insulating film of the capacitor;

forming a second polysilicon layer and an upper electrode of the capacitor from the second polysilicon layer, wherein the first dielectric layer covers a region of the first polysilicon layer at which PN junctions of the lateral polysilicon diodes are to be formed; and

forming a resist mask, for injecting ions into an N-type region of the lateral polysilicon diode and for injecting ions into a P-type region of the lateral polysilicon diode, on the first dielectric layer.

10. (Amended) A method of manufacturing a high-frequency semiconductor device having a MOS transistor, lateral polysilicon diodes, and a capacitor on a substrate, and a first of the lateral polysilicon diodes connects a high-frequency I/O signal line to an externally supplied voltage, VDD, and a second of lateral polysilicon diodes connects ground, GND, to the high-frequency I/O signal line, the method comprising:

forming a first polysilicon layer and a lower electrode of the capacitor and the lateral polysilicon diodes from the first polysilicon layer:

forming a first dielectric layer as an insulating film of the capacitor;

A39

forming a second polysilicon layer and an upper electrode of the capacitor from the second polysilicon layer, wherein the second polysilicon layer covers a region of the first polysilicon layer at which PN junctions of the lateral polysilicon diodes are to be formed; and

forming a resist mask, for injecting ions into an N-type region of the lateral polysilicon diode and for injecting ions into a P-type region of the lateral polysilicon diode, on the second polysilicon layer.

11. (Amended) The manufacturing method of claim 9, including forming a gate electrode of the MOS transistor from the second polysilicon layer.

12. (Amended) The high-frequency semiconductor device of claim 1 further comprising a clamp circuit connected between the externally supplied voltage, VDD, and ground, GND, wherein the clamp circuit permits current flow at a voltage lower than a reverse bias breakdown voltage of the first lateral polysilicon diode.

Add C4